

# FDH45N50F

## N-Channel UniFET™ FRFET® MOSFET

500 V, 45 A, 120 mΩ

### Features

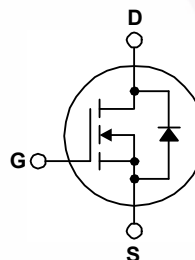
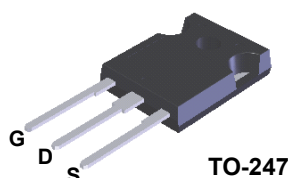
- $R_{DS(on)} = 105 \text{ m}\Omega$  (Typ.) @  $V_{GS} = 10 \text{ V}$ ,  $I_D = 22.5 \text{ A}$
- Low Gate Charge (Typ. 105 nC)
- Low  $C_{rss}$  (Typ. 62 pF)
- 100% Avalanche Tested
- Improved dv/dt Capability

### Applications

- Lighting
- Uninterruptible Power Supply
- AC-DC Power Supply

### Description

UniFET™ MOSFET is Fairchild Semiconductor's high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on-state resistance, and to provide better switching performance and higher avalanche energy strength. The body diode's reverse recovery performance of UniFET FRFET® MOSFET has been enhanced by lifetime control. Its  $t_{rr}$  is less than 100nsec and the reverse dv/dt immunity is 15V/ns while normal planar MOSFETs have over 200nsec and 4.5V/nsec respectively. Therefore, it can remove additional component and improve system reliability in certain applications in which the performance of MOSFET's body diode is significant. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts



### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter		FDH45N50F_F133	Unit
$V_{DSS}$	Drain-Source Voltage		500	V
$I_D$	Drain Current	- Continuous ( $T_C = 25^\circ\text{C}$ )	45	A
		- Continuous ( $T_C = 100^\circ\text{C}$ )	28.4	A
$I_{DM}$	Drain Current	- Pulsed (Note 1)	180	A
$V_{GSS}$	Gate-Source voltage		$\pm 30$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)		1868	mJ
$I_{AR}$	Avalanche Current (Note 1)		45	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)		62.5	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		50	V/ns
$P_D$	Power Dissipation	( $T_C = 25^\circ\text{C}$ )	625	W
		- Derate Above $25^\circ\text{C}$	5	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range		-55 to +150	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds		300	$^\circ\text{C}$

### Thermal Characteristics

Symbol	Parameter	FDH45N50F_F133	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	0.2	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	40	

## Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDH45N50F_F133	FDH45N50F	TO-247	Tube	N/A	N/A	30 units

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max	Unit
Off Characteristics						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	500	--	--	V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C	--	0.5	--	V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 500 V, V <sub>GS</sub> = 0 V V <sub>DS</sub> = 400 V, T <sub>C</sub> = 125°C	-- --	-- --	25 250	μA μA
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 30 V, V <sub>DS</sub> = 0 V	--	--	100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = -30 V, V <sub>DS</sub> = 0 V	--	--	-100	nA
On Characteristics						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	3.0	--	5.0	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 22.5 A	--	0.105	0.12	Ω
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 40 V, I <sub>D</sub> = 22.5 A	--	49.0	--	S
Dynamic Characteristics						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, f = 1 MHz	--	5100	6630	pF
C <sub>oss</sub>	Output Capacitance		--	790	1030	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		--	62	--	pF
C <sub>oss</sub>	Output Capacitance	V <sub>DS</sub> = 400 V, V <sub>GS</sub> = 0 V, f = 1 MHz	--	161	--	pF
C <sub>oss(eff.)</sub>	Effective Output Capacitance	V <sub>DS</sub> = 0 V to 400 V, V <sub>GS</sub> = 0 V	--	342	--	pF
Switching Characteristics						
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 250 V, I <sub>D</sub> = 48 A, V <sub>GS</sub> = 10 V, R <sub>G</sub> = 25 Ω	--	140	290	ns
t <sub>r</sub>	Turn-On Rise Time		--	500	1010	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		--	215	440	ns
t <sub>f</sub>	Turn-Off Fall Time		(Note 4) --	245	500	ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> = 400 V, I <sub>D</sub> = 48 A, V <sub>GS</sub> = 10 V	--	105	137	nC
Q <sub>gs</sub>	Gate-Source Charge		--	33	--	nC
Q <sub>gd</sub>	Gate-Drain Charge		(Note 4) --	45	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current		--	--	45	A
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current		--	--	180	A
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 45 A	--	--	1.4	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 45 A, dI <sub>F</sub> /dt =100 A/μs	--	188	--	ns
Q <sub>rr</sub>	Reverse Recovery Charge		--	0.64	--	μC

### Notes:

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2.  $L = 1.46\text{ mH}$ ,  $I_{AS} = 48\text{ A}$ ,  $V_{DD} = 50\text{ V}$ ,  $R_G = 25\text{ }\Omega$ , starting  $T_J = 25^\circ\text{C}$ .
3.  $I_{SD} \leq 45\text{ A}$ ,  $dI/dt \leq 200\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq BV_{DSS}$ , starting  $T_J = 25^\circ\text{C}$ .
4. Essentially independent of operating temperature typical characteristics.

## Typical Performance Characteristics

Figure 1. On-Region Characteristics

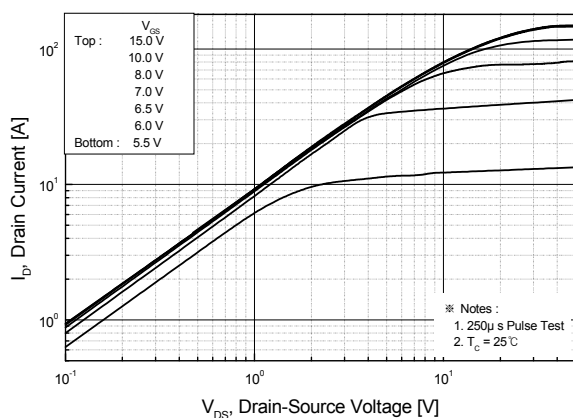


Figure 2. Transfer Characteristics

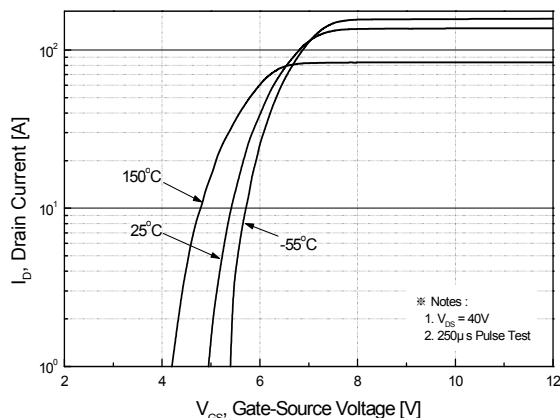


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

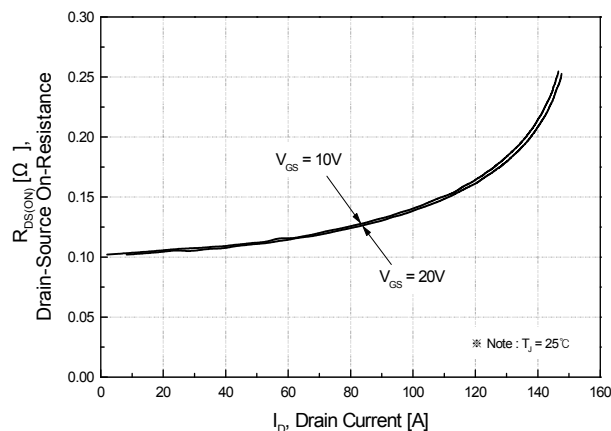


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

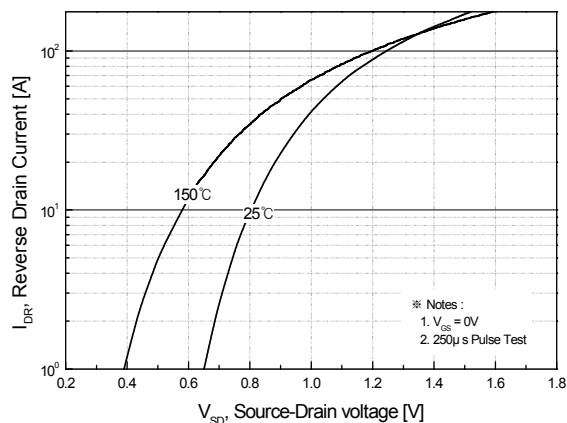


Figure 5. Capacitance Characteristics

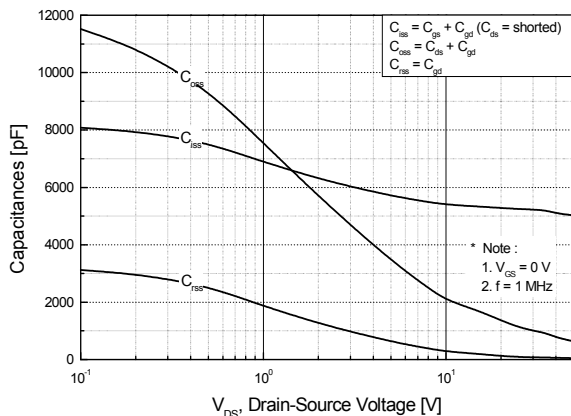
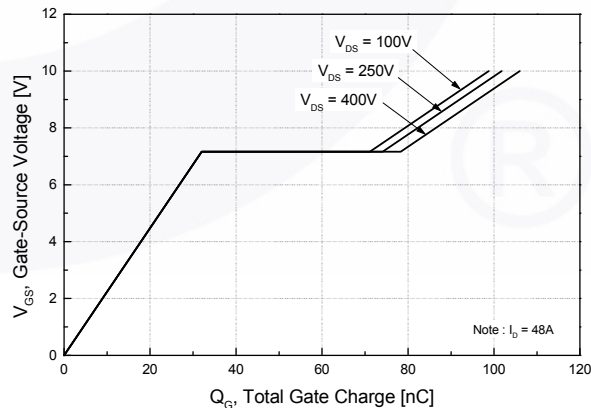
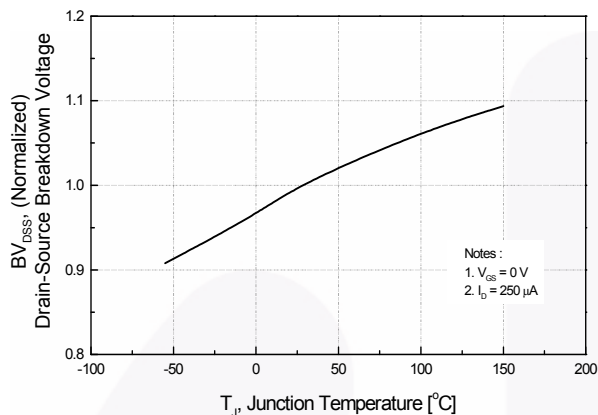


Figure 6. Gate Charge Characteristics

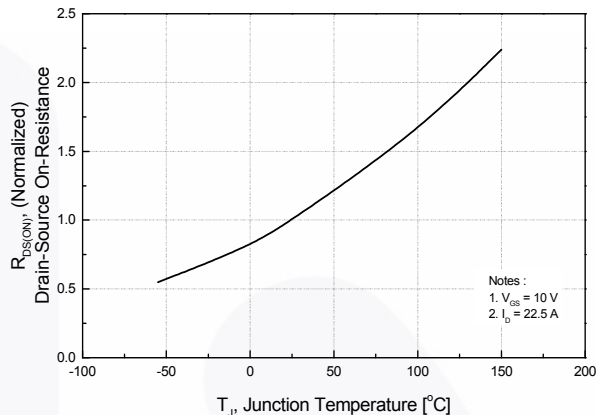


## Typical Performance Characteristics (Continued)

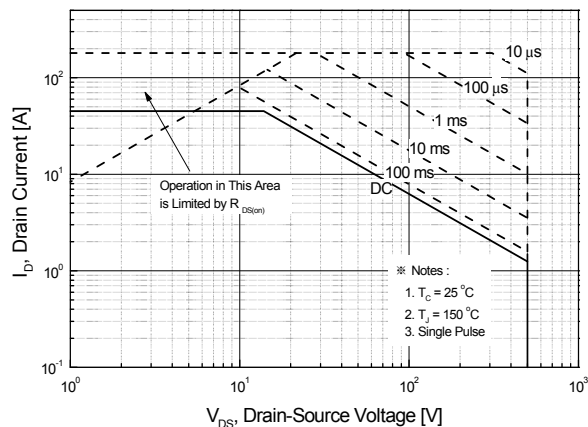
**Figure 7. Breakdown Voltage Variation vs. Temperature**



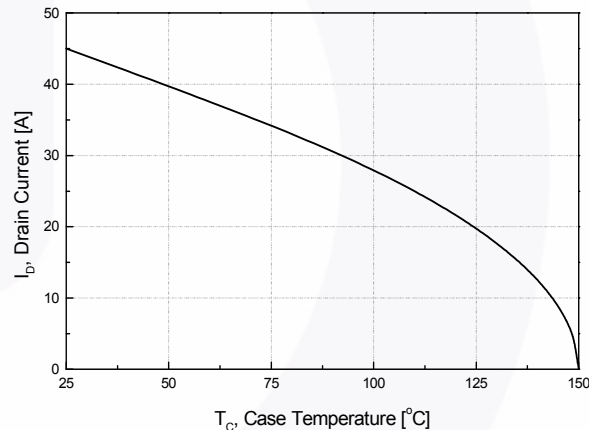
**Figure 8. On-Resistance Variation vs. Temperature**



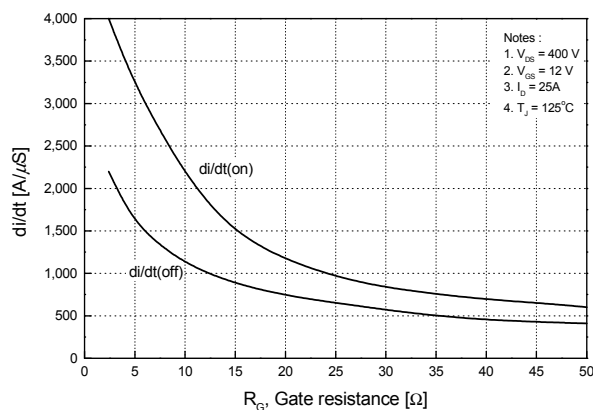
**Figure 9. Maximum Safe Operating Area**



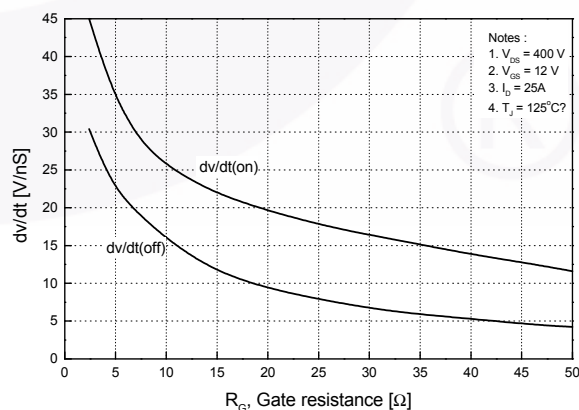
**Figure 10. Maximum Drain Current vs. Case Temperature**



**Figure 11. Typical Drain Current Slope vs. Gate Resistance**



**Figure 12. Typical Drain-Source Voltage Slope vs. Gate Resistance**



## Typical Performance Characteristics (Continued)

Figure 13. Typical Switching Losses vs. Gate Resistance

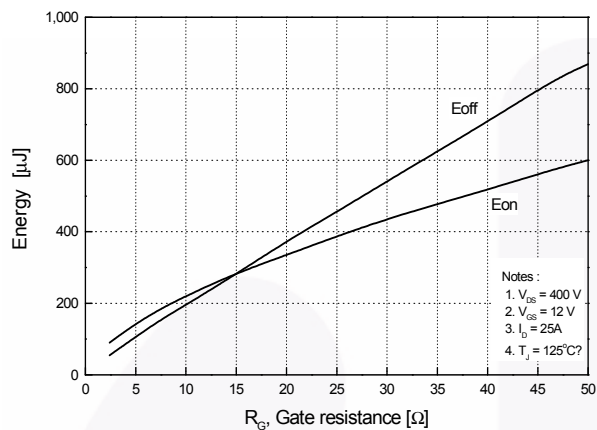


Figure 14. Unclamped Inductive Switching Capability

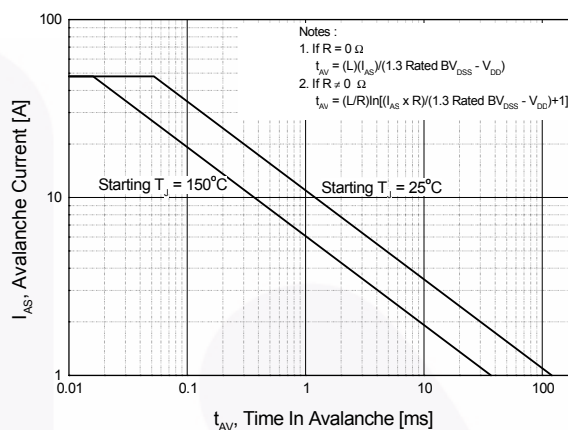
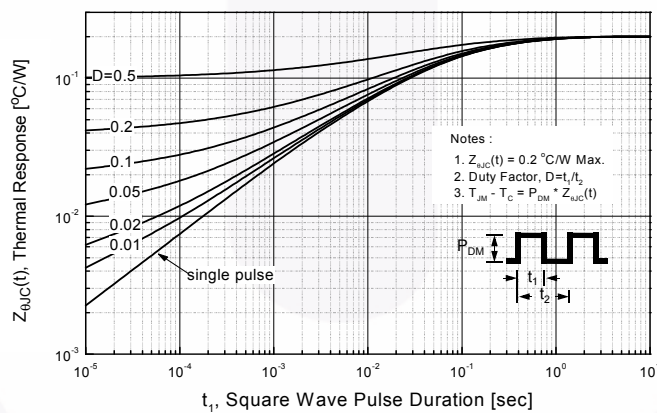


Figure 15. Transient Thermal Resistance Curve



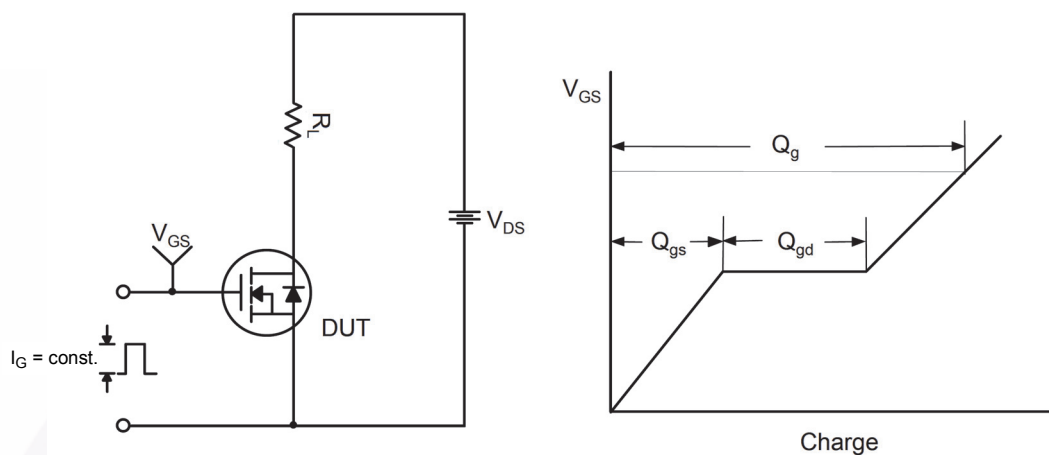


Figure 16. Gate Charge Test Circuit & Waveform

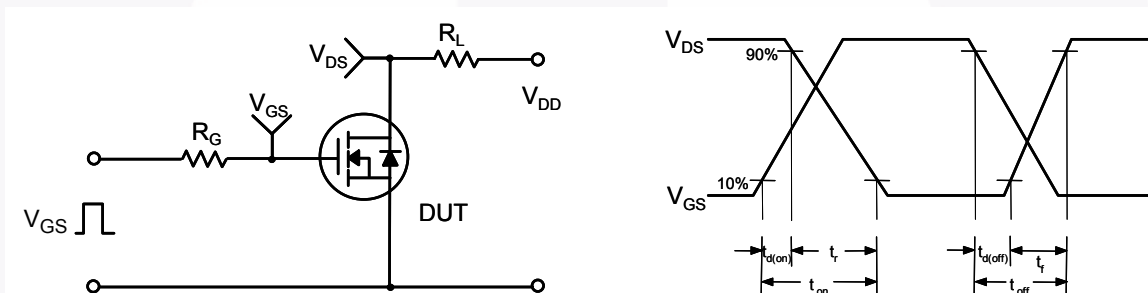


Figure 17. Resistive Switching Test Circuit & Waveforms

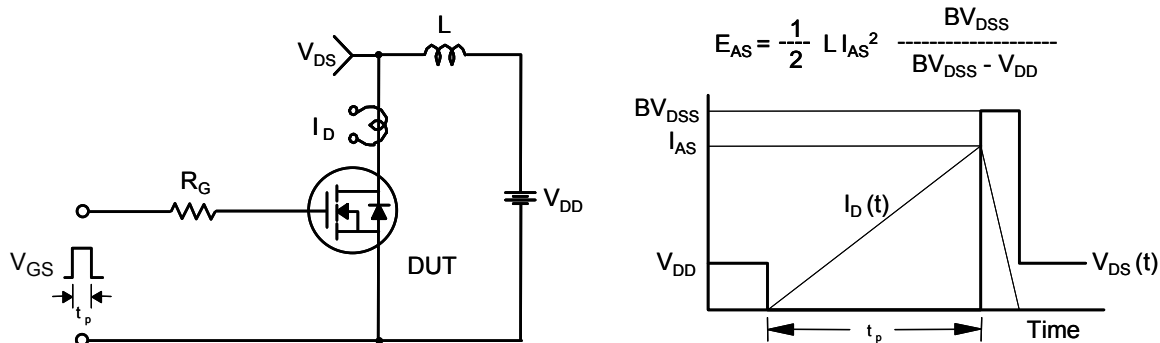
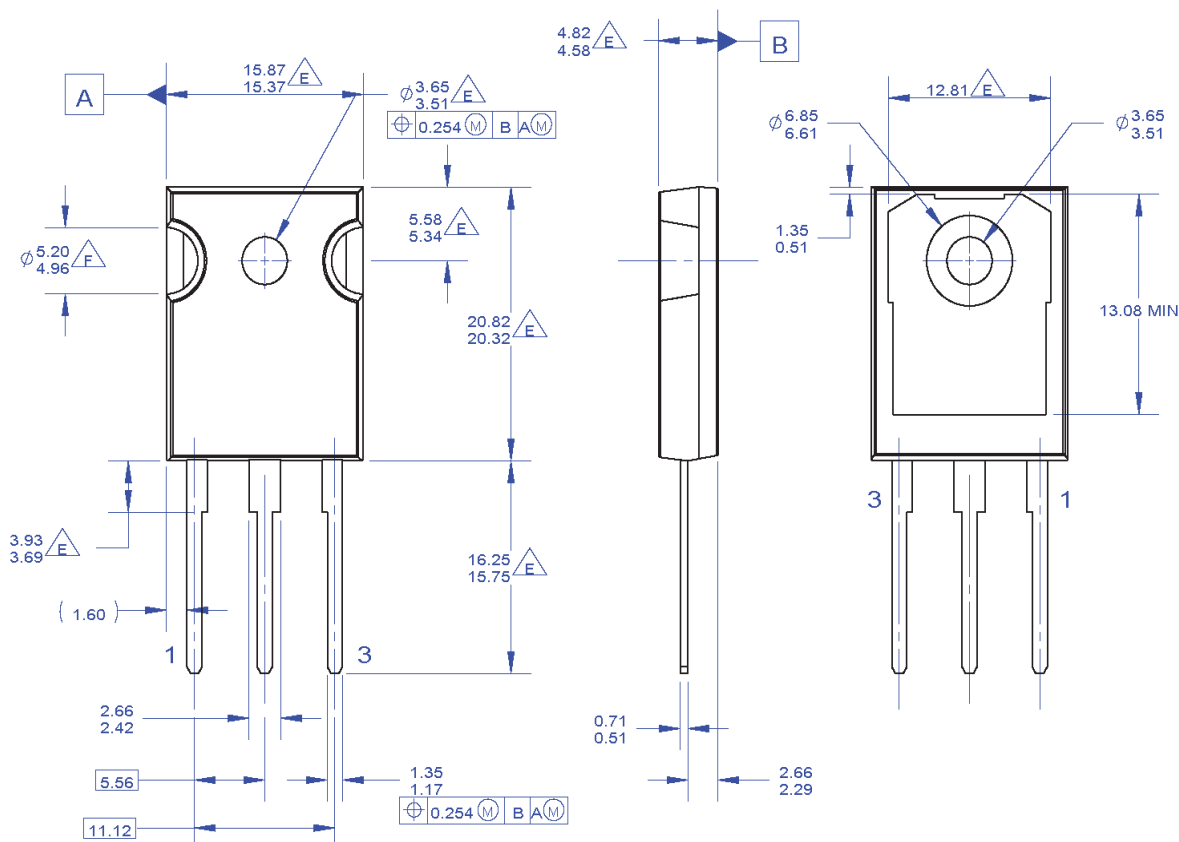


Figure 18. Unclamped Inductive Switching Test Circuit & Waveforms



Figure 19. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms

## Mechanical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED.

- A. PACKAGE REFERENCE: JEDEC TO-247, ISSUE E, VARIATION AB, DATED JUNE, 2004.
- B. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DRAWING CONFORMS TO ASME Y14.5 - 1994

$\triangle E$  DOES NOT COMPLY JEDEC STANDARD VALUE

$\triangle F$  NOTCH MAY BE SQUARE

G. DRAWING FILENAME: MKT-TO247A03\_REV03

**Figure 20. TO-247, Molded, 3-Lead, Jedec Variation AB**

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Datasheet Identification	Product Status	Definition
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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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Rev. I66

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